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FORM PTO-1449 #4

FORM PTO-1449	SERIAL NO. 09/972,787	CASE NO. 10519/37
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE October 5, 2001	GROUP ART UNIT 2185
(use several sheets if necessary)	APPLICANT(S): Friedman et al.	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES	NO

EXAMINER INITIAL		OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
U/E	A1	"64M x 8 Bit NAND Flash Memory," Samsung Electronics (October 27, 2000).	
U/E	A2	"How Flash Memory Works," wysiwyg://8/http://www.howstuffworks.com/flash-memory.htm?printable=1, 5 pages (1998).	✓
U/E	A3	"Datalight FlashFX™ 4.06 User's Guide," page 11 (August 2000).	
U/E	A4	"How Does TrueFFS® manage Wear Leveling?," http://www.m-sys.com/content/information/calcInfo.asp, 2 pages (printed October 5, 2001)	

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EXAMINER Kevin L. Ellis	DATE CONSIDERED 5/23/03

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uk	A1	5,414,829	05/1995	Fandrich et al.		

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
UR	A1	6,181,603	01/30/2001	Jyouno et al.		
UR	A2	6,034,882	03/07/2000	Johnson et al.		
KE	A3	6,236,587	05/22/2001	Gudesen et al.		
UR	A4	6,363,008	03/2002	Wong		
UR	A5	6,219,282	04/2001	Tanaka		
UR	A6	6,376,282	04/2002	Corisis		
UR	A7	6,222,762	04/2001	Guterman et al.		
UR	A8	6,151,246	11/2000	So et al.		
UR	A9	6,134,141	10/2000	Wong		
UR	A10	5,264,740	11/1993	Wright		
UR	A11	5,153,462	10/1992	Agrawal et al.		
UR	A12	6,376,284	04/2002	Gonzalez et al.		

EXAMINER INITIAL		OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
UR	A13	"Intel StrataFlash™ Memory Technology Development and Implementation," Fazio et al., Intel Technology Journal, 13 pages (Q4'1997).
UR	A14	"A 125mm^2 1Gb NAND Flash Memory with 10MB/s Program Throughput," Nakamura et al., ISSCC 2002/Session 6/SRAM and Non-Volatile Memories/6.4, 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 106-107 (2002).
UR	A15	"On the Go With Sonos," White et al., Circuits & Devices, pages 22-31 (July 2000).
KE	A16	"NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," Eitan et al., IEEE Electron Device Letters, Vol. 21, No. 11, pages 543-545 (November 2000).
UE	A17	"A 512Mb NROM Flash Data Storage Memory with 8MB/s Data Rate," Maayan et al., ISSCC 2002/Session 6/SRAM and Non-Volatile Memories/6.1, 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 100-101 (2002).
UR	A18	"Ovonic Unified Memory – A High-Performance Nonvolatile Memory Technology for Stand-Alone Memory and Embedded Applications," Gill et al., ISSCC 2002/Session 12/TD Digital Directions/12.4, 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 202-203 (2002).
UR	A19	"0.13 μm Metal-Oxide-Nitride-Oxide-Semiconductor Single Transistor Memory Cell with Separated Source Line," Fujiwara et al., Jpn. J. Appl. Phys. Vol. 39, pp. 417-423, Part 1, No. 2A (February 2000).
UR	A20	"Three-Dimensional Memory Array and Method of Fabrication," U.S. Patent Application Serial No. 09/560,626, filing date 04/28/2000, inventor: N. Johan Knall.

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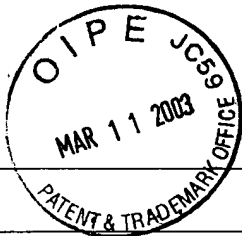|		
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UR	A21	"Digital Memory Method and System for Storing Multiple-Bit Digital Data," U.S. Patent Application Serial No. 09/932,701, filing date 08/17/2001, inventors: Michael A. Vyvoda and N. Johan Knall.
UR	A22	"Memory Device and Method for Reliably Reading Multi-Bit Data from a Write-Many Memory Cell," U.S. Patent Application Serial No. 10/144,451, filing date 5/9/02, inventor: Bendik Kleveland.

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uk	A1	6,278,633 B1	08/2001	Wong et al.		

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